NAMIBIA UNIVERSITY
OF SCIENCE AND TECHNOLOGY

FACULTY OF COMPUTING AND INFORMATICS
DEPARTMENT OF COMPUTER SCIENCE

QUALIFICATION: BACHELOR OF COMPUTER SCIENCE, BACHELOR OF COMPUTER IN CYBER SECURITY & BACHELOR OF INFORMATICS	
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COURSE: COMPUTER ORGANISATION AND ARCHITECTURE	**COURSE CODE**: COA511S
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DURATION: 2H	**MARKS:** 100

FIRST OPPORTUNITY EXAMINATION QUESTION PAPER	
EXAMINER(S)	MR. JULIUS SILAA MS. JOVITA MATEUS MS. VICTORIA SHAKELA MS. HELENA HAINANA MR. THOMAS SHOMWELE
MODERATOR:	MR. SIMON MUCHINENYIKA

THIS QUESTION PAPER CONSISTS OF 6 PAGES
(Excluding this front page)

INSTRUCTIONS

1. Answer ALL the questions on the answer scripts.
2. Write clearly and neatly.
3. Number the answers clearly.

PERMISSIBLE MATERIALS

1. Calculator.

SECTION A [15 MARKS]: Each Question Weighs 1 Mark.

1. The CMOS battery on the motherboard stores BIOS settings of the computer. [True/False]
2. The ALU (Arithmetic Logic Unit) is one of the components of a CPU. [True/False]
3. The first major change in the electronic computer came with the replacement of the transistor with a vacuum tube. [True/False]
4. Organizational attributes include hardware details transparent to the programmer. [True/False]
5. The speed of a processor is dictated by the pulse frequency produced by the clock, measured in cycles per second, or Hertz (Hz). [True/False]
6. The I/O function includes a control and timing requirement, to coordinate the flow of traffic between internal resources and external devices. [True/False]
7. Pipelining is a means of introducing parallelism into the essential sequential nature of a machine-instruction program. [True/False]
8. Addition and subtraction can be performed on numbers in two complement notation by treating them as unsigned integers. [True/False]
9. Although convenient for computers, the binary system is exceedingly cumbersome for human beings. [True/False]
10. In the Direct Memory Access (DMA) mode, the I/O module and main memory exchange data directly, without processor involvement. [True/False]
11. Hexadecimal notation is more compact than binary notation. [True/False]
12. In a system without virtual memory, the effective address is a virtual address or a register. [True/False]
13. Segmentation is usually visible to the programmer and is provided as a convenience for organizing programs and data and as a means for associating privilege and protection attributes with instructions and data. [True/False]
14. Instruction pipelining is a powerful technique for enhancing performance but requires careful design to achieve optimum results with reasonable complexity. [True/False]
15. The XOR operator yields false if both its operands are False. [True/False]

SECTION B [15 MARKS]: Each Question Weighs 1 Mark.

1. A _____ is a mechanism that provides for communication among CPU, main memory, and I/O.

A. system interconnection B. CPU interconnection

C. peripheral D. processor

2.The _____ defines the third generation of computers.

A. integrated circuit B. vacuum tube

C. D. VLSI

3. A line includes a _____ that identifies which particular block is currently being stored.

A. Cache B. hit C. tag D. locality

4. A variety of errors can occur while a computer system is running. When that happens, the OS must make a response that clears the error condition with the least impact on running applications. The OS takes care of these errors through the _____ service.

A. Error correction and response B. Error correcting

C. Error responsiveness D. Error detection and response

5. _____ is implemented with combinational circuits.

A. Nano memory B. Random access memory

C. Read only memory D. No memory

6. Which properties do all semiconductor memory cells share?

A. They exhibit two stable states which can be used to represent binary 1 and 0

B. They are capable of being written into to set the state

C. They are capable of being read to sense the state

D. All of the above

7. The most fundamental type of machine instruction is the _____ instruction.

A. conversion B. data transfer

C. arithmetic D. logical

8. Binary 0101 is hexadecimal _____.

A. 0 B. 5

C. A D. 10

9.The decimal system is said to have a base, or radix, of _____.

A. 10 B. 16

C. 2 D. 4

10. In any number, the leftmost digit is referred to as the _____.

A. lease significant digit B. a most common digit

C. most significant digit D. least common digit

11. The _____ determines the opcode and the operand specifiers.

A. decode instruction B. fetch operands

C. calculate operands D. execute instruction

12. The operand _____ yields true if either or both of its operands are true.

A. NOT B. AND

C. NAND D. OR

13. _____ instructions provide computational capabilities for processing number data.

A. Boolean B. Logic

C. Memory D. Arithmetic

14. A _____ is a dispatch able unit of work within a process that includes a processor context and its own data area for a stack.

A. Process B. Process switch

C. Thread D. Thread switch

15. Which of the following interrelated factors go into determining the use of the addressing bits?

A. number of operands
B. number of register sets
C. address range
D. all of the above

SECTION C [70 MARKS]: Comprehension questions.

Question 1

a) List and briefly explain one distinctive achievement of generation two (1950s) and generation three (1960s) of computers. (4 marks)

b) The von Neumann architecture, which is also known as the Von Neumann model and Princeton architecture, is a computer architecture based on the 1945 description by the mathematician and physicist John von Neumann and others in the First Draft of a Report on the EDVAC.

Briefly explain his three main ideas (You may alternatively give an answer in a form of a well labeled diagram). (6 marks)

Question 2

a) Referencing memory pyramid, outline any four categories of memory provided in a digital computer? (4 marks)

b) Registers are fast stand-alone storage locations that hold data temporarily in CPU.

List any three types of registers and explain their functions. (6 marks)

c) Cache memory, also called CPU memory, is random access memory (RAM) that a computer microprocessor can access more quickly than it can access regular RAM.

This memory is typically integrated directly with the CPU chip or placed on a separate chip that has a separate bus interconnect with the CPU.

List and briefly describe three cache mapping schemes (6 marks)

Question 3

a) Briefly describe any four attributes of a computer form factor. (8 marks)

b) CPU is a precious computer resource and a good computing system should be design in such way to utilize CPU efficiently. Explain why DMA is better than interrupt-driven and Programmed I/O in terms of CPU usage. (5 marks)

Question 4

a) Give any two examples of each of the following types of digital circuits (4 marks)

i) Combinational
ii) Sequential

b) Explain one major difference between Combinational and Sequential circuits. (3 marks)

c) Why does the program execution speed generally increase as the number of general purpose registers increase? (4 marks)

Question 5

a) The Main Memory consist of 128 MB, and suppose this memory is word addressable meaning that every word has its own unique address for accessing it.

b) Compute the number of addressable words in this memory (4 marks)

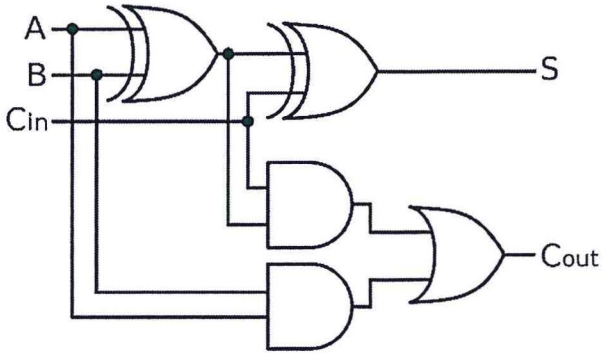
c) Suppose this memory is divided into fixed length of 64 words each How many blocks are in this memory? (2 marks)

d) How many lines of cache memory will be required to accommodate all blocks of main memory in 3b above by using the direct cache addressing scheme? (2 marks)

Question 6

a) List any 4 types of basic logical gates (2 marks)

b) Identify(name) the following combinational circuit found in the ALU. (2 marks)



c) Draw a truth table depicting the circuit above. As shown in the diagram above your truth table should include three inputs and two outputs. Remember the output depend on the types of gate shown in the circuit. (8 marks)

*******END OF PAPER*******